REMARKS

The claims now pending in the application are Claims 1, 2, 4 to 7, 9 and 10, the independent claims being Claims 1 and 7. Claims 3 and 8 have been cancelled. Claims 1, 5, 7 and 10 have been amended.

In the Official Action dated April 14, 2003, the specification was objected to on formal grounds. Claim 3 was objected to on formal grounds. Claims 7 to 10 were rejected under 35 U.S.C. § 112, second paragraph, as indefinite. Claims 1, 3 and 4 were rejected under 35 U.S.C. § 102(b), as anticipated by U.S. Patent No. 5,854,950 (Handa), and Claims 2, 3 and 5 to 10 variously were rejected under 35 U.S.C. § 103(a), as unpatentable over the Handa '950 patent in view of one or more of U.S. Patent No. 5,942,877 (Nishimura), U.S. Patent No. 4,825,233 (Kanai) and Japanese Patent Publication No. 06-250278 (Kitani). Reconsideration and withdrawal of the objections and the rejections respectfully are requested in view of the above amendments and the following remarks.

The formal objection to the specification respectfully is traversed. Applicant submits that those skilled in the art readily will understand the recited features of "a time-keeping clock signal generation circuit" and "a ferroelectric memory time-keeping counter circuit", as disclosed and claimed in the present application. In this regard, Applicant notes that each of these features relates to a *circuit* (e.g., a ferroelectric memory circuit), as illustrated, e.g., in Fig. 1 and described in the corresponding written disclosure.. Reconsideration and withdrawal of the formal rejections respectfully are requested.

The formal rejection of Claims 7 to 10 respectfully is traversed. Nevertheless, without conceding the propriety of the rejection, Claim 7 has been amended herein to clarify the claim language and obviate the formal rejection. No new matter has been added.

The rejections of the claims over the cited prior art respectfully are traversed. Nevertheless, without conceding the propriety of the rejections, Claims 3 and 8 have been canceled and Claims 1, 5, 7 and 10 have been amended herein more clearly to recite various novel features of the present invention. Support for the proposed amendments may be found in the original disclosure. No new matter has been added.

The present invention relates to a novel electronic apparatus. In one aspect, as now recited in independent Claim 1, the present invention relates to an electronic apparatus comprising a clock circuit that generates a clock signal having clock signal pulses generated at a predetermined cycle, a non-volatile memory time-keeping counter circuit, and a control circuit that controls the electronic apparatus, wherein the clock signal pulses generated by the clock circuit are input to the control circuit, and the control circuit outputs the clock signal pulses to the non-volatile memory time-keeping circuit so as to count the clock signal pulses generated by the clock circuit and store a count of the clock signal pulses in the non-volatile memory time-keeping counter circuit.

In another aspect, as now recited in independent Claim 7, the present invention relates to an electronic apparatus comprising a time-keeping clock signal generation circuit that keeps time, a ferroelectric memory time-keeping counter circuit, and a control circuit that controls the electronic apparatus, wherein the time kept by the time-keeping clock signal generation circuit is input to the control circuit, and the control circuit outputs the time to the

ferroelectric memory time-keeping counter circuit such that the ferroelectric memory time-keeping counter circuit forms and stores a time signal concerning time kept by the time-keeping clock signal generation circuit.

Thus, as discussed in greater detail in the present application, in each aspect a non-volatile memory time-keeping circuit (or ferroelectric memory time-keeping counter circuit) is used to perform counting/storing based on a signal from a clock circuit (or time-keeping clock signal generation circuit) processed through a control circuit (e.g., a central processing unit CPU).

Applicant submits that the prior art fails to anticipate the present invention. Moreover, Applicant submits that there are differences between the subject matter sought to be patented and the prior art, such that the subject matter taken as a whole would not have been obvious to one of ordinary skill in the art at the time the invention was made.

The Handa '950 patent relates to a data recording device for a camera and film type camera with lens, and discloses a data recording device capable of preventing the recording of incorrect date and time data on photographic film due to malfunction of the time counter that generates date and time data for recording. A drive of the data recording device has a time counter that generates date and time data for recording. The count value of the date and time data generated by this time counter are stored in a storage circuit. However, Applicant submits that the Handa '950 patent fails to disclose or suggest at least the above-described features of the present invention. In particular, Applicant understands the Handa '950 patent arrangement merely to teach that clock pulses are counted in a time counter 161 and that the count value of the time counter is stored in a storage circuit 33 separate from the time counter. Further,

immediately prior to the operation that changes the count value of the time counter, the date and time data in the storage circuit and the counter value of the date and time data from the time counter are compared in a comparison judgment circuit. If the two do not agree, a malfunction detection signal which indicates that the time counter has malfunctioned is output to the driver and the recording of date and time data by liquid crystal display panel is stopped. Applicant submits that the Handa '950 patent fails to disclose or suggest at least the feature of using a non-volatile memory time-keeping circuit (or ferroelectric memory time-keeping counter circuit) to count and store a signal from a clock circuit (or clock signal generation circuit), as disclosed and claimed in the present application.

The Nishimura '877 patent relates to a portable information device and charger therefor, and is cited for its alleged teaching that a ferroelectric RAM and an EEPROM may be used interchangeably. However, without conceding the propriety of the Examiner's characterization, Applicant submits that the Nishimura '877 patent fails to disclose or suggest at least the above-described features of the present invention. Applicant submits that the Nishimura '877 patent fails to disclose or suggest at least the feature of using a non-volatile memory time-keeping circuit (or ferroelectric memory time-keeping counter circuit) to count and store a signal from a clock circuit (or clock signal generation circuit), as disclosed and claimed in the present application. Nor is the Nishimura '877 patent believed to add anything to the Handa '950 patent that would make obvious the claimed invention.

The Kanai '233 patent relates to a data recording camera, and was cited for its teaching of a camera having a clock circuit and a corresponding memory circuit. However, Applicant submits that the Kanai '233 patent fails to disclose or suggest at least the above-

discussed features of the present invention. Nor is the Kanai '233 patent understood to add anything to the Handa '950 patent and/or the Nishimura '877 patent that would make obvious the claimed invention.

The Kitani JP '278 reference relates to camera apparatus, and was cited for its teaching of a nonvolatile memory circuit that starts counting a state in which a predetermined value is added to the memory contents of the nonvolatile memory circuit when a power supply (power cell 43) for supplying power to the camera is replaced for eliminating the need for a backup supply voltage. However, Applicant submits that the Kitani JP '278 reference fails to disclose or suggest at least the above-discussed features of the present invention. Nor is the Kitani JP '278 reference understood to add anything to the Handa '950 patent, the Nishimura '877 patent and/or the Kanai '233 patent that would make obvious the claimed invention.

A review of the other art of record has failed to reveal anything which, in Applicant's opinion, would remedy the deficiencies of the art discussed above, as references against the independent claims herein. Those claims are therefore believed patentable over the art of record.

For the above reasons, Applicant submits that Claims 1 and 7 are allowable over the cited art.

Claims 2, 4 to 6, 9 and 10 depend from Claims 1 and 7, respectively, and are believed allowable for the same reasons. Moreover, each of these dependent claims recites additional features in combination with the features of its respective base claim, and is believed allowable in its own right. Individual consideration of the dependent claims respectfully is requested.

Applicant submits that the present Amendment is fully responsive to each of the points raised by the Examiner in the Official Action, and that the Application is in condition for allowance. Favorable consideration of the claims, and passage to issue of the application at the Examiner's earliest convenience earnestly are solicited.

Applicant's undersigned attorney may be reached in our Washington, D.C. office by telephone at (202) 530-1010. All correspondence should continue to be directed to our below listed address.

Respectfully submitted,

Attorney for Applicant

Registration No. 32,078

FITZPATRICK, CELLA, HARPER & SCINTO
30 Rockefeller Plaza
New York, New York 10112-3801
Facsimile: (212) 218-2200
CPW\gmc

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